APPLICATION NOTE

PIP3 TOPFETs for industrial automation

AN01048

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1 INTRODUCTION

Following on from the success of the ‘BUK***’ TOPFETs, Philips Semiconductors continues to expand its range of ‘PIP3***’ Temperature and Overload Protected Field Effect Transistors (TOPFETs). This product line is based on and developed from the ‘BUK***’ TOPFETs, which are aimed principally at automotive applications. The PIP3 TOPFETs, however, suit the resistive and inductive loads found in most process control, factory automation and battery powered equipment used in industry.

This application note introduces the TOPFET, its functions and the benefits it lends to industrial automation applications. Also included are the rules that should be followed to get your TOPFET application working first time, every time, whatever the load.

2 DEFINITION

A TOPFET is a low voltage power MOSFET with dedicated on-chip protection circuits. It has all the advantages of a conventional power MOSFET (low R_{DSon}, logic level gate drive) with the additional benefits of integrated protection from overstress conditions and the provision of output indication of device status. TOPFETs are available as low side and high side types.

3 LOW SIDE TYPE (‘PIP31**’)

Low side TOPFETs and associated drive signals are referenced to the ground line. The load is permanently connected to the positive supply and the negative supply to it is switched via the low side TOPFET switch.

Figure 1 shows a simplified circuit diagram of a 5-pin low side TOPFET. This device has a separate pin for the logic power supply. Keeping input and logic supply separate gives more flexibility in the specification of the internal series gate resistance; lower resistance allows faster switching. R_{IG} for 5-pin low side TOPFETs is typically 1.7 kΩ, making them suitable for linear operation and high speed switching up to 20 kHz.

3-pin low side TOPFETs are also available (see Fig.2) in which the logic power supply is derived from the input signal. They can be used as plug-in replacements for conventional MOSFETs to provide added protection features.

Because their input and logic supply share a common pin, R_{IG} must be high (typically 33 kΩ) in order to maintain the logic supply during latched fault conditions. 3-pin low side TOPFETs are therefore best suited to low slew rate switching of DC loads up to a maximum frequency of 400 to 500 Hz.

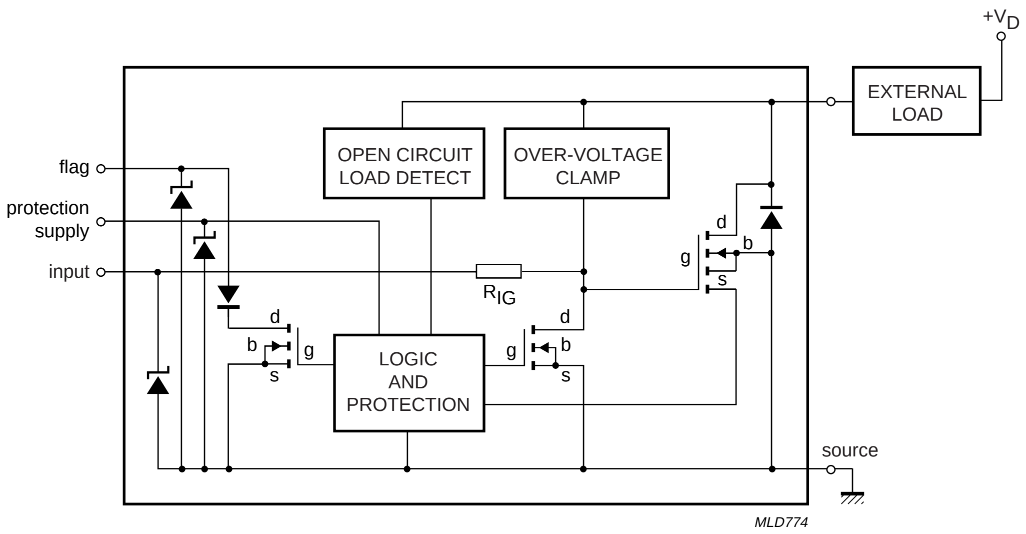

Fig.1 5-pin low side TOPFET; simplified circuit diagram.

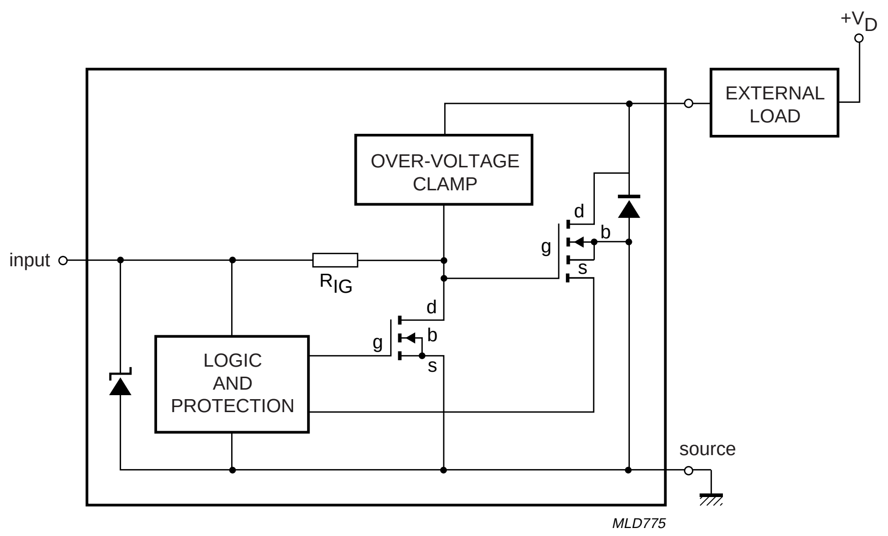

Fig.2 3-pin low side TOPFET; simplified circuit diagram.

4 LOW SIDE QUICK REFERENCE DATA

SYMBOL	PARAMETER	UNIT	DETAILS
	pin designations		drain, input, source, flag (5-pin types), protection supply (5-pin types)
V_{DS}	continuous drain-source voltage	V	determined by clamp voltage. At the time of writing, the minimum limit for all types is 50 V
I_D	continuous drain current	A	theoretical limits with device mounting base temperature (T_{mb}) held at 25 °C
P_D	total power dissipation	W	
T_j	continuous junction temperature	°C	set by minimum trip temperature $T_{j(TO)}$ to 150 °C minimum
R_{DSon}	drain-source on-state resistance	mΩ	the most important specification and the starting point for TOPFET design-in

5 HIGH SIDE TYPE (‘PIP32**’)

High side TOPFETs are connected to the positive supply, although associated drive signals are still referenced to the ground line in the normal way. The load is permanently connected to ground and the positive supply to it is switched via the high side TOPFET switch.

Built-in level shift circuitry provides interfacing between the ground-referenced input and the positive supply-referenced output MOSFET.

At the time of writing, the internal level shift and charge pump circuitry of high side TOPFETs cannot support high speed switching. These types are therefore best suited to low slew rate switching of DC loads up to a maximum frequency of 400 to 500 Hz.

Dual high side TOPFETs are also available in which both output MOSFET channels share a common protection circuit.

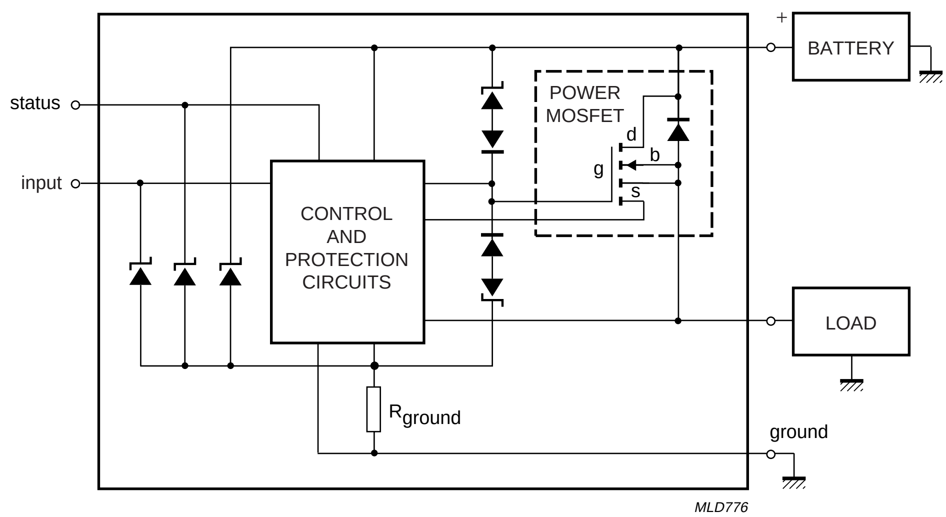

Fig.3 5-pin high side TOPFET; simplified circuit diagram.

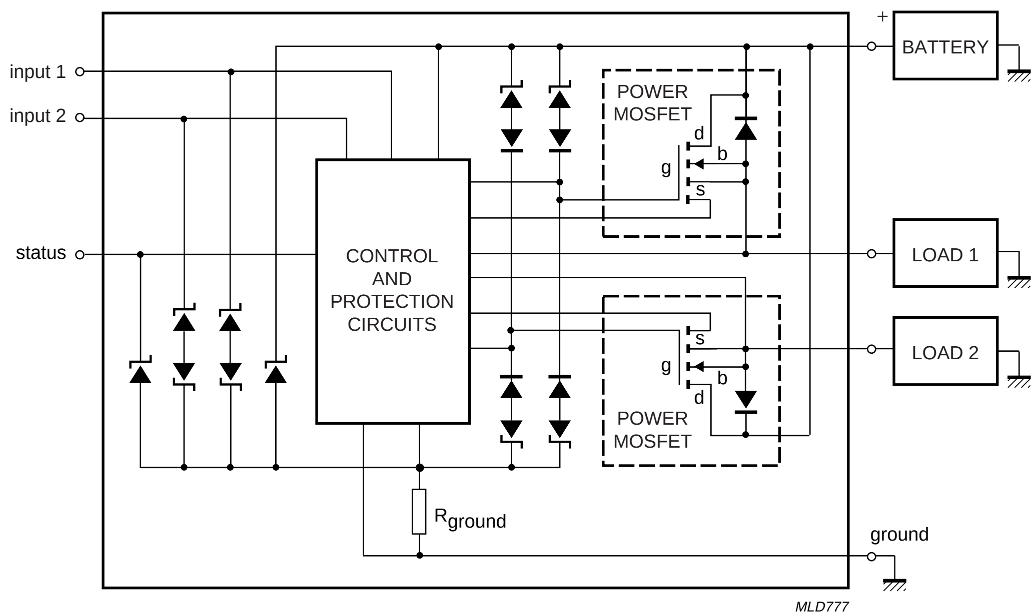

Fig.4 Dual high side TOPFET; simplified circuit diagram.

6 HIGH SIDE QUICK REFERENCE DATA

SYMBOL	PARAMETER	UNIT	DETAILS
	pin designations		battery, input, load, status and ground
V_{BG}	continuous off-state supply voltage	V	battery-ground voltage is determined by clamp voltage. At the time of writing, the minimum limit for all types is 50 V
I_L	minimum nominal load current (ISO)	A	minimum current to produce a battery-load voltage (V_{BL}) of 0.5 V at T_{mb} = 85 °C
I_L	maximum continuous load current	A	theoretical limit with device mounting base temperature (T_{mb}) held at 25 °C
T_j	continuous junction temperature	°C	set by minimum trip temperature $T_{j(TO)}$
R_{on}	on-state resistance (T_j = 25 °C)	mΩ	the most important specification and the starting point for TOPFET design-in

7 PROTECTION STRATEGIES

7.1 Over-temperature protection

Over-temperature conditions are often relatively slow acting (measured in seconds) because they result from poor heat sinking or marginal over-current. When the TOPFET temperature exceeds the threshold junction temperature $T_{j(TO)}$ the output MOSFET is shut down to prevent damage and to allow recovery. Response time can be many seconds for marginal faults or less than 100 µs for a hard fault. A feature of the TOPFET is on-chip absolute temperature detection which is an integral part of over-temperature detection. There are two forms of over-temperature protection, latched or unlatched.

7.1.1 LATCHED PROTECTION

Latched protection requires user reset by toggling the input pin low (3-pin low side and high side TOPFETs) or by toggling the protection supply pin low (5-pin low side TOPFETs).

7.1.2 UNLATCHED PROTECTION

Unlatched protection provides auto reset, whereby the TOPFET resumes normal operation after the device temperature has fallen below the trip temperature.

7.2 Short circuit protection

A short circuited load causes very rapid rise in the MOSFET junction temperature. This condition must be detected within milliseconds to protect the output MOSFET from a localised melt-down. One of two detection methods is used: thermal or electrical.

7.2.1 THERMAL METHOD

The thermal method employs on-chip differential temperature detection. The energy dissipation due to a short circuited load causes a steep temperature gradient between the output MOSFET and its control circuit. Two temperature sensors adjacent to the MOSFET, one closer than the other, monitor temperature. The imbalance arising from the high thermal gradient is detected by a bridge circuit whose output is used to turn off the MOSFET. Response time is dependent on the type of fault condition and ranges from less than 90 µs to over 2 ms.

7.2.2 ELECTRICAL METHOD (HIGH SIDE ONLY)

The electrical method detects battery-load voltage. The MOSFET drain-source voltage is monitored and compared with a pre-defined battery-load threshold voltage ($V_{BL(TO)}$). A built-in delay allows the normal turn-on sequence to complete before the detection system is armed. Once armed, the output MOSFET can be deactivated within 10 µs of a fault being detected.

Note: $V_{BL(TO)}$ is approximately two thirds V_{BG} to ensure tracking of the trip threshold with the supply voltage. This avoids premature tripping with higher supply voltages, as would occur if the threshold were optimized and fixed for a 12 V system.

Short circuit protection is latched. The TOPFET is reset by toggling the input pin low (3-pin low side and high side) or by toggling the protection supply pin low (5-pin low side).

7.3 Over-current protection

Over-current protection limits fault current to a pre-defined maximum in the event of a short circuit. Now fitted as standard to all TOPFETs, it protects the customer's circuits and wiring while removing the inconvenience of blown fuses. It is factory adjustable to suit application requirements.

7.4 Transient over-voltage and ESD protection

The TOPFET includes circuitry which protects the chip from over-voltage, voltage transients arising from the turn-off of unclamped inductive loads and electrostatic discharge (ESD).

The inclusion of a network between the drain and gate of the output MOSFET prevents it from going into avalanche breakdown by partially turning the MOSFET on when the voltage rise is too great. The MOSFET subsequently conducts sufficiently to clamp the voltage to a safe level.

Voltage clamps between the supply terminals of the logic circuits and ground provide protection to these circuits. ESD protection diodes are fitted to all other terminals.

Low side TOPFETs are protected from transients due to the turn-off of an inductive load by over-voltage-clamping circuitry.

In a high side TOPFET, the transient starts driving the load pin level below ground. Should this exceed a pre-defined negative voltage it is clamped by a network between the ground pin and the MOSFET gate which partially turns on the MOSFET. This voltage is factory adjustable to suit application requirements.

7.5 Reverse supply protection

The output MOSFET will not be damaged if the power supply connections to the TOPFET are reversed. This is due to the fact that the current flow is conducted via the body drain diode and is limited by the load.

The internal ground resistor R_G on high side types limits the ground-to-battery current to a safe level.

7.6 Flag/status

The Flag/status output indicates that the TOPFET has been tripped by an over-temperature, overload or short circuit condition. It can also indicate that the protection supply is absent. It is an open drain output and should be connected to an external pull-up resistor with a value of 47 to 100 kΩ.

7.7 Open circuit detection

An open circuit may be detected by onboard circuitry either sensing low current in the on state or by sensing high load resistance in the off state.

7.8 Loss of ground connection

High side TOPFETs shut down immediately if the connection to ground is broken.

8 DRIVING TOPFETS

The output of a TOPFET is similar to that of a power MOSFET. The TOPFET’s protection features, however, make its input characteristics significantly different to those of a MOSFET gate.

8.1 Low side TOPFET (5-pin)

8.1.1 INPUT REQUIREMENTS

- Input voltage must always be positive with respect to the source.
- Input voltage should be within the input-source voltage range - i.e. for logic 1, above the maximum threshold voltage $V_{IS(TO)}$ and below the minimum input-source clamping voltage $V_{(CL)IS}$; for logic 0, below the minimum $V_{IS(TO)}$.
- Input-source current I_{IS} is 100 µA maximum. With overload protection latched, the low series input resistance means that input current (I_{ISL}) can rise to 4 mA maximum if the driver can source it. It is not necessary, however, to source this level of clamping current. A high resistance driver will simply be pulled down during clamping. This is perfectly acceptable.

8.1.2 INPUT DRIVER OPTIONS

The input can be driven directly from any driver with high or low output resistance.

Note: All TOPFETs have sufficient input pull-down to ensure turn off in the event of an input open circuit.

8.1.3 PROTECTION SUPPLY REQUIREMENTS

- Protection supply voltage must always be positive with respect to the source.
- During normal operation, the protection supply voltage should be above the maximum threshold voltage V_{PSF} and below the minimum clamping voltage $V_{(CL)PS}$.
- To reset an ‘overload protection latched’ condition, the protection supply must be less than the minimum specified reset voltage V_{PSR} for a duration of at least the maximum reset time t_{pr}.
- Protection supply current during normal operation or when latched (I_{PS} and I_{PSL}) is 450 µA maximum.

8.1.4 PROTECTION SUPPLY DRIVER OPTIONS

- The preferred driver is a logic gate; this will satisfy the protection supply current requirements and permit toggling low to reset (see Fig.5).
- The protection supply can be derived directly from the 5 V logic supply. This, however, requires the removal of power to reset a trip condition. Connection to 5 V via a pull-up resistor of 3 kΩ allows a transistor pull-down for resetting (see Fig.6).

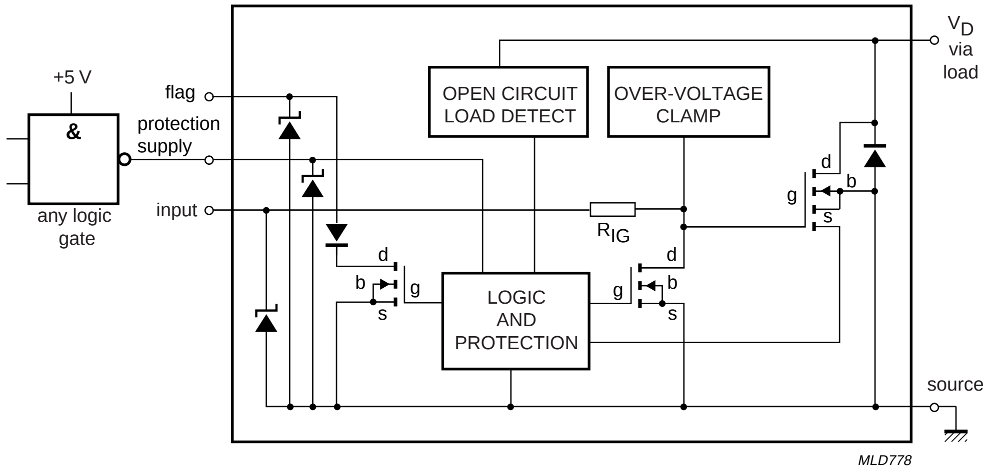

Fig.5 Protection supply from logic gate.

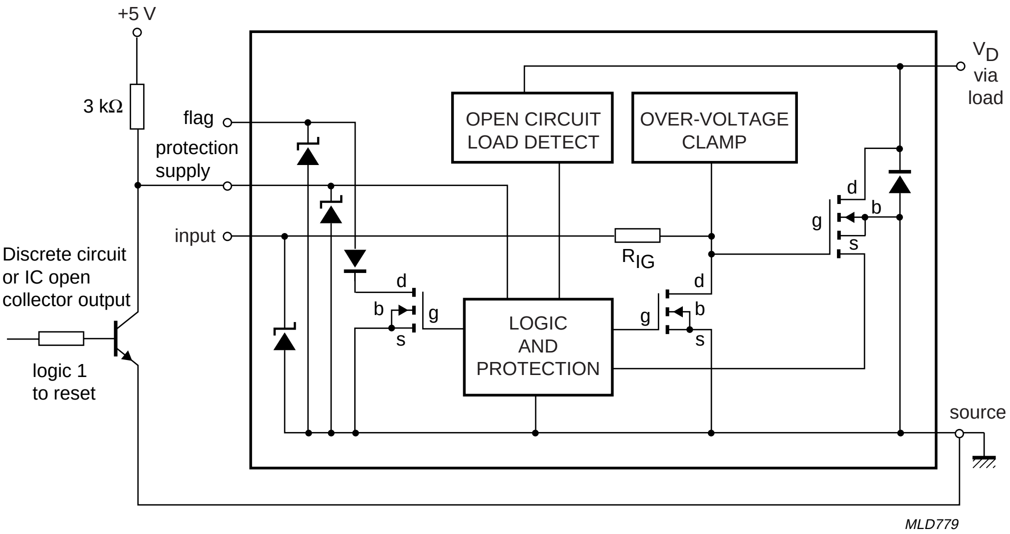

Fig.6 Protection supply from open collector output.

8.2 Low side TOPFET (3-pin)

8.2.1 INPUT REQUIREMENTS

- Rules for input voltage are the same as for the 5-pin device.
- During normal operation, the input-source current I_{IS} is 400 µA maximum. This is a combination of input current and logic supply current. When the overload protection has been tripped, the input current I_{ISL} will rise to a level dictated by the input resistance R_{IG}. R_{IG} can be changed by the factory, the higher its resistance, the lower the current. With the standard 33 kΩ, I_{ISL} would be 430 µA maximum at V_{IS} = 3 V. The driver must be able to maintain this voltage while supplying I_{ISL} in order to maintain logic supply integrity and ensure that the TOPFET stays properly latched off.

8.2.2 INPUT DRIVER OPTIONS

- A microcontroller output port can satisfy the input requirements of the standard TOPFETs with an input resistance of 33 kΩ (see Fig.7)
- A complementary push-pull driver, either a CMOS IC gate or discrete, will be required if a device with lower R_{IG} is specified to give increased switching speed (see Fig.8).

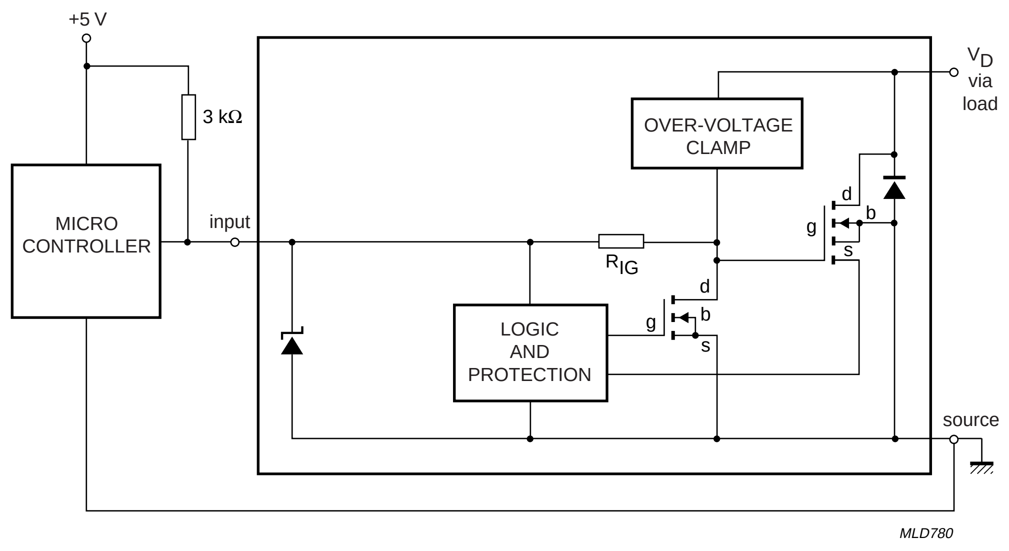

Fig.7 Low current microcontroller driver for high resistance inputs.

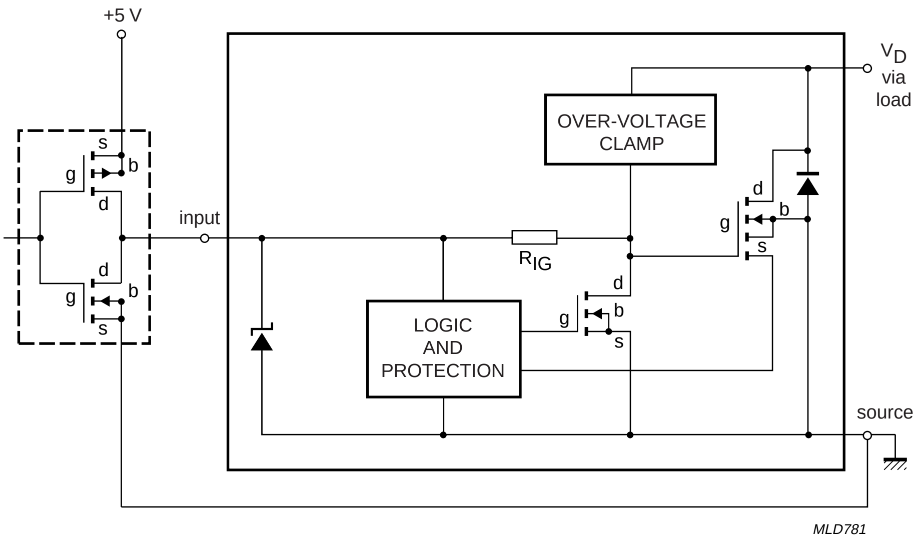

Fig.8 Push-pull driver for faster switching of low resistance inputs.

8.3 High side TOPFET

8.3.1 INPUT REQUIREMENTS

The logic input is subject to the threshold voltages specified in data:

- Logic 1: input-ground voltage should be above the maximum input turn-on threshold voltage $V_{IG(ON)}$ and below the minimum input-ground clamping voltage V_{IG}.
- Logic 0: input-ground voltage should be below the minimum turn-off threshold voltage $V_{IG(OFF)}$
- Input current I_I is 160 µA maximum.

8.3.2 INPUT DRIVER OPTIONS

Input can be driven directly from any driver with high output resistance - e.g. a microcontroller output port.

The logic power is taken from the battery pin, the return current exiting via the ground pin.

Note: when turned off with a logic 0 on the input, high side TOPFETs shut down and draw quiescent current of 20 µA maximum from the supply. This includes leakage current through the load.

9 TOPFET LOADS

9.1 Resistive - heater

This is a simple load with no issues of concern, since the maximum current with cold element is only marginally higher than the current for a hot element.

9.2 High inrush resistive - incandescent lamp

The resistance of a cold incandescent lamp filament is very low compared to that of a hot filament; 200 mΩ being a typical value. TOPFETs will operate in current limit mode until the filament has heated and current demand has fallen below the limit current. This is perfectly acceptable.

While current limiting, TOPFETs operate in linear mode and can dissipate high power. Depending on starting temperature, power dissipation, current limit level, heat sinking arrangement and the duration of limiting, the TOPFET might reach a power dissipation trip condition (low side and dual high side types) or an over-temperature trip condition (high side types). One or two reset operations can be attempted to get through the lamp warm-up phase and into normal running. It is not good practice, however, to resort to this method too many times in quick succession. If two reset operations cannot achieve normal operation, one or more of the following system changes should be made:

- Reduce the ambient temperature prior to the inrush event.
- If the TOPFET is operating shortly before an inrush event, select a larger device with lower MOSFET on-resistance to reduce power dissipation, hence reduce the starting temperature.
- Reduce the junction-to-ambient thermal resistance by improving heat sinking.
- If more than one lamp is controlled by one TOPFET, reduce the number of lamps to reduce the duration of limiting.

9.3 Inductive - motor

A TOPFET-controlled motor will most likely be a DC permanent magnet brush motor whose stall current can be expected to be two to three times the running current. Long-term stall conditions are covered by the TOPFET's over-temperature protection.

When the TOPFET turns off, the brief inductive kickback is not severe and is easily handled by the TOPFET voltage transient protection. The reverse (generator) current that follows afterwards will flow through the body drain diode of the output MOSFET. This remains the case even if the motor is mechanically overdriven.

9.4 Inductive - solenoid valve, contactor coil

Solenoid and contactor coils have very high inductance with very high unclamped turn-off energy. ('Unclamped' refers to the absence of a freewheel diode in anti-parallel with the load.)

The very nature of inductive load clamping prevents the TOPFET from being able to turn off the output MOSFET; it must continue to conduct until the inductive load current has decayed naturally.

While clamping at 50 V minimum, the output MOSFET must conduct the clamping current. High power dissipation is the result. Excessive energy resulting from too much current for too long will cause the silicon to melt and the device to be destroyed. For this reason, it is necessary to quote a maximum permissible inductive load clamping energy in data. Because this is a thermal issue, the energy is quoted under specific conditions of junction temperature: the higher the starting T_j, the lower the clamping energy capability.

As long as the clamping energy remains below the maximum permitted value for the TOPFET, it is not necessary to include a freewheel diode across the load. For large inductive loads, however, where there is a risk of exceeding the TOPFET's clamping energy rating, a freewheel diode should be fitted.

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